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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/694,237 | 10/27/2003 | Kayvan Sadra | TI-35961 | 2682 |

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| EXAMINER | |
|---|---|
| SCHILLINGER, LAURA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | |

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/694,237 | SADRA ET AL. | |
| | Examiner | Art Unit | |
| | Laura M. Schillinger | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *13-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/03*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *1/18/05* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Claims 13-28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 1/10/05 and 1/18/05 (See interview Summary).

Applicant's traversal of the restriction requirement made on 1/18/05 is considered untimely.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Dennison ('176).

1. A method of fabricating a semiconductor device comprising:

forming first type well regions within a core logic portion and an embedded memory portion of the device (Fig.2 (104 and 102) and Col.5, lines: 30-40);

forming second type well regions within the core logic portion and the embedded memory portion of the device (Fig. 2 (104, 102) and Col.4, lines: 20-30);

performing a supplemental isolation implant within at least one of the first type well regions of the embedded memory portion to modify dopant profiles of the at least one of the first type well regions to increase isolation(Col.5, lines: 5-15.

2. The method of claim 1, further comprising performing a supplemental isolation implant within at least one of the second type well regions to modify dopant profiles of the at least one of the second type well regions to increase isolation (Col.5, lines: 5-15).

3. The method of claim 2, wherein the first type well regions are n-type and the second type well regions are p-type (Col.5, lines: 30-40 and Col.4, lines: 20-30).

4. The method of claim 2, wherein the first type well regions are p-type and the second type regions are n-type (Col.4, lines: 20-30 and Col.5, lines: 30-40).

5. The method of claim 1, further comprising forming first shallow trench isolation regions having a first width that separate active regions across well boundaries within the core logic portion and forming second shallow trench isolation regions having a second width that separate active regions across well boundaries within the embedded memory portion (Col.s 6-7, lines: 55-45).

6. The method of claim 5, wherein the second width is less than the first width (Col.s 6-7, lines: 55-45).

7. The method of claim 5, wherein the second width is substantially less than the first width (Col.s 6-7, lines: 55-45).

8. The method of claim 1 , further comprising forming stacked gate structures prior to performing a supplemental isolation implant (Fig.2 (134)).

9. The method of claim 1, wherein performing a supplemental isolation implant within the first type well regions of the embedded memory portion comprises: forming a layer of resist on the device and selectively exposing the first type well regions of the embedded memory; and implanting one or more dopants of the first type into the exposed first type well regions (Fig.3).

10. The method of claim 9, wherein the layer of resist formed is also employed to raise a threshold voltage of high-threshold-voltage transistors formed on the device (inherent- doping will adjust threshold voltage when performed in the active region as shown in Fig.3).

11. The method of claim 10, wherein the threshold voltage of the high- threshold-voltage transistors is raised using a channel implant (Fig.3- inherent- doping will adjust threshold voltage when performed in the active region).

12. The method of claim 10, wherein the threshold voltage of the high- threshold-voltage transistors is raised using a pocket implant (Fig.15 (231 inherent- doping will adjust threshold voltage when performed in the active region).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMS

1/20/05